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MODELING AND TESTING OF FAULTS IN 2TG1M MEMRISTOR MEMORIES

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ABSTRACT

Recently, memristor memory has drawn attention as an attractive option for future non-volatile memories due to its high density, low power consumption and long retention time. However, memristor memory has high defect density due to its nanoscale fabrication and it also suffers from sneak path problem owing to its crossbar architecture. In this paper, fault models for 2TG1M (2 Transmission Gates and 1 Memristor) memory are proposed. A new fault Write Disturbance Fault is analyzed. Additionally, a March Test is proposed to cover the defined faults. The proposed March test requires 5mn read and 5mn write operations for mxn (m words x n bits) 2TG1M memory.

KEYWORDS: Memristor, Test, Fault Models

I. INTRODUCTION

Memristor is a concatenation of ‘memory resistor’ and has the characteristics of both of them. It is a nonlinear device whose memristance (measured in Ohms) is a function of the electric charge that has passed through the device. Memristors have a variety of applications such as non-volatile memory, programmable logic, neuromorphic systems, etc. owing to its scalability, low power consumption and dynamic response.

Moore's Law [1] will eventually cease to exist as CMOS technologies are shrinking, with devices attaining dimensions comparable to their constituting atoms [2]. Thus, the focus has to be shifted in finding devices, which are increasingly infinitesimal and equally if not more capable than the transistors. Memristors are an attractive option for next generation memory architectures due to their high density, long retention time, and low power operation.

In a metal oxide Memristor memory the resistance between its terminals is used to represent the two logic states, logic 0 and logic 1. Memristor memory array can be simply designed as crossbar architecture in which only a single memristor connects to the wordline and the bitline. However, it suffers with the problem of sneak-path. In order to reduce sneak path several biasing techniques have been proposed [3] [4]. As array size increases these techniques fail since they do not eliminate sneak path current. To eliminate sneak path problem another technique in which a selector device is connected with the memristor at each node can be used. Selector device may be a diode, transistor, transmission gate. With diode only unipolar memristor can be used. The use of pass transistor in the memristor memory array decreases potential difference across the memristor thereby causing reduction in speed of charge carriers flowing through the memristor. Also, one transistor one memristor (1T1M) memory cell requires a bipolar voltage application for its writing process [5]. In 2TG1M memory cell both high and low logic levels are passed through the memristor effectively without any noticeable voltage drop across the transmission gate device. Also it takes advantage of bidirectional capabilities of transmission gates and memristor.

Several researchers have discussed memristor defects, their fault models and March elements to detect those faults. Most of the faults in memristor occur due to parametric variation of the device. In [6], fault models for memristor (1M) are proposed and March algorithm for efficient testing is described.

In this paper, an electrical fault modelling for 2TG1M memristor memories is performed by analysing transistor stuck-open, stuck-on, bridge, and open defects. Moreover, the bridge defects between neighbouring cells are considered. Additionally, a test algorithm is proposed to detect the defined faults. The remaining paper is organized as follows. Section II briefly reviews the memristor and 2TG1M memristor memory. Section III presents electrical defects in 2TG1M memory and their fault models. Section IV introduces the proposed march test for the defined faults. Finally, Section V concludes this paper.

II. MEMRISTOR AND 2TG1M MEMRISTOR MEMORY

1. Memristor

The concept of memristor was first proposed by Leon Chua in 1971 who postulated that mathematically a fourth circuit element could exist [7]. The memristor, with memristance M provides a functional relation between charge and flux, $d\Phi=Mdq$. The Metal oxide memristor developed in 2008 by HP labs [8] consists of an active region made up of thin film of titanium oxide (TiO_2) sandwiched between two platinum electrodes. The TiO_2 film is D nm long and contains two regions- TiO_2 (D-w nm) and TiO_{2-x} (w nm). The TiO_2 region has low conductivity and TiO_{2-x} (oxygen deficient titanium oxide or doped with oxygen vacancies) has high conductivity. An essential attribute of this device is that the resistances of doped and undoped regions differ significantly. Thus, the overall resistance of the device may be viewed as series combination of two resistances. The overall resistance depends on the state variable of memristor, α ($0\leq \alpha \geq 1$) which is defined as the ratio of length of doped region to the total length of memristor. When positively biased voltage ($v(t)>0$) is applied across the memristor, the oxygen vacancies drift to the TiO_2 region thus decreasing the overall resistance of memristor. On the contrary, application of negatively biased voltage across the memristor increases its resistance. The rate of drift is non-linear in both directions. A fully doped memristor has lowest possible resistance denoted by R_{on}. Similarly, a fully undoped memristor has highest possible resistance denoted by R_{off}.

The overall memristance (M) of memristor is given by

$$M(\alpha) = \alpha R_{on} + (1-\alpha) R_{off}$$

The logic levels are defined according to the memristance value which is calculated by measuring current flowing through the memristor. For ideal case, if current flowing through the memristor is greater than Iref (reference current) then value stored in memristor is considered as logic 1 and if current is less than Iref then logic 0 is considered. To ensure the reliability of memristor by mitigating the effect of noise, the upper and lower threshold currents Ion, Ioff are defined. Logic 1 is defined as the region where current flowing through memristor is greater than Ion. Similarly, if current flowing through memristor is less than Ioff then it is considered as logic 0. On the other hand, if the current through memristor is in between Ion and Ioff then it is undefined region which may randomly be considered as logic 1 or logic 0.

2. 2TG1M MEMRISTOR MEMORY

Figure 1 shows a 2TG1M memory cell consisting of a transistor and two transmission gates. The one bit memory cell is controlled by two data lines (DATA and $\overline{\text{DATA}}$) and two write lines (WRITE and $\overline{\text{WRITE}}$). The two data lines

are complement of one another and similar is the case with two write lines. Data line provides the data to be written and write line is used to select the memory cell in which data is to be written or from which data is to be read. WRITE is connected to the gate terminal of NMOS and $\overline{\text{WRITE}}$ is connected to gate terminal of PMOS in transmission gate. DATA is connected to the positive terminal of memristor via transmission gate, while $\overline{\text{DATA}}$ is connected to the negative terminal of the memristor via another identical transmission gate. The purpose of using $\overline{\text{DATA}}$ is to maintain the potential difference across the memristor equal to VCC whenever the cell is writing enabled.

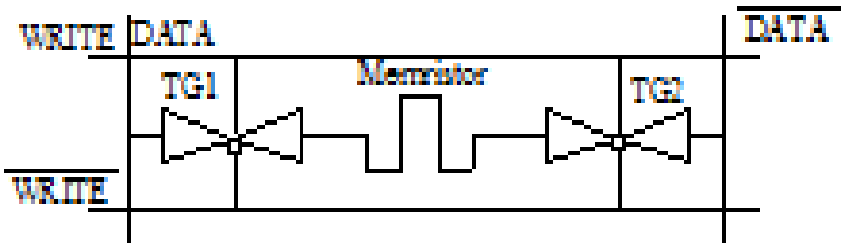

Figure 1: 2TG1M memory cell

2.1 Write Operation

To write in a 2TG1M memory cell, it is selected by applying V_{CC} to WRITE. To write a '1' into the 2TG1M memory cell, DATA is charged to V_{CC} and $\overline{\text{DATA}}$ will be grounded. It results in positive potential at the positive terminal of memristor while the negative terminal is grounded, which causes the substrate layer to be doped by vacancies thereby resulting in a low resistance conducting channel. This creates path for high current flow. Thus, memristor is said to be written with logic '1' due to low memristance value.

To write a '0' into the 2TG1M memory cell, DATA is grounded and $\overline{\text{DATA}}$ is charged to VCC which results in voltage at negative terminal of memristor greater than that at its positive terminal. Thus, oxygen vacancies decrease resulting in high memristance of memristor. Hence, the logic value becomes '0'.

2.2 Read Operation

For reading operation a very short duration write pulse is applied, which turns on both the transmission gates on either side of memristor, thereby selecting the memristor for read operation. The duration of this write pulse must be a fraction of writing time of memristor in order to maintain the state of memristor. For this duration a negative pulse followed by a positive pulse is applied at DATA and a positive pulse followed by a negative pulse is applied at $\overline{\text{DATA}}$ [9]. The magnitude of current flowing through the memristor indicates the logic level stored in memristor irrespective of its direction.

2.3 2TG1M mxn Memory

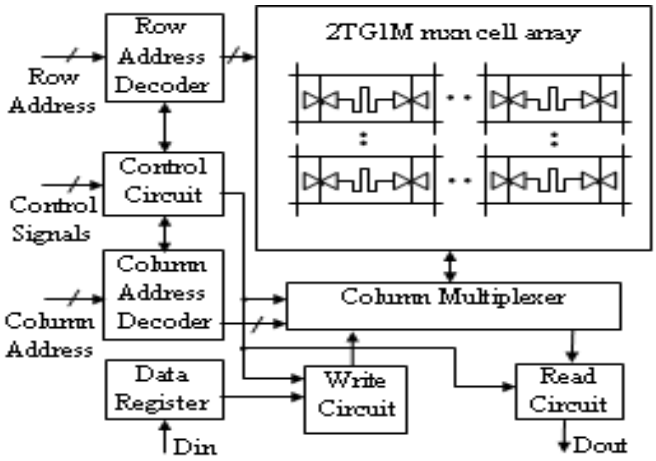

Figure 2: Block Diagram of mxn 2TG1M Memory

Block diagram of 2TG1M mxn memory is shown in fig. 2. In the 2TG1M memory cell array, the cells in same row share WRITE and $\overline{\text{WRITE}}$, and cells in same column share DATA and $\overline{\text{DATA}}$. When a read or write operation is performed then the peripheral read and write circuit associated with the array, generates the signals required at write and data lines. The peripheral shown in figure is similar to that in conventional memory.

III.ELECTRICAL DEFECTS AND FAULT MODELS

1. Electrical Defects

Following electrical defects are examined to analyse possible fault behaviours of 2TG1M memristor memory.

- **Defects in memristor**
  - Variation in doping
  - Variation in length
  - Variation in area
- **Defects in transmission gate**
  - Transistor stuck-open
  - Transistor stuck-on
- **Defects in connecting wires**
  - Open: represents unwanted resistance between connections.
  - Bridge: represents short between cells or lines.

Various bridging defects possible in 2TG1M memory are given in Table 1. 2x2 2TG1M memristor array given in figure 3 is considered to analyze these defects.

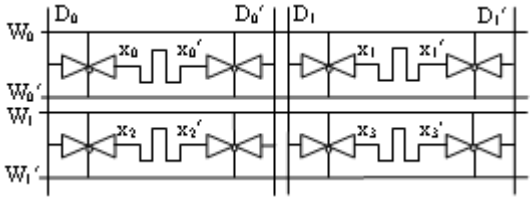

Figure 3: 2x2 2TG1M Memory Array

Table 1: Possible Bridge Defects in 2 x 2 2TG1M Memory

Bridge	Location	Bridge	Location
R_{B1}	W_0-W_1'	R_{B12}	D_0-D_1'
R_{B2}	W_0'-W_1'	R_{B13}	D_0'-D_1
R_{B3}	W_0-W_0'	R_{B14}	D_0'-D_1'
R_{B4}	W_0'-W_1	R_{B15}	x_0-W_1
R_{B5}	W_0'-x_0	R_{B16}	x_0-D_1
R_{B6}	W_0'-x_0'	R_{B17}	x_0-W_1'
R_{B7}	W_0-D_0	R_{B18}	x_0-D_1'
R_{B8}	W_0-D_0'	R_{B19}	x_0'-W_1
R_{B9}	W_0'-D_0	R_{B20}	x_0'-D_1
R_{B10}	W_0'-D_0'	R_{B21}	x_0'-W_1'
R_{B11}	D_0-D_1	R_{B22}	x_0'-D_1'

2. Fault Models

- **Faults Caused by Memristor Defects**
  - **Stuck-at-1:** It is caused due to excessive doping of oxygen vacancies in substrate. This fault also occurs if memristor is shorted to Vdd.
  - **Stuck-at-0:** If the memristor is undoped, then s-a-0 fault occurs. It may also occur if memristor is shorted to ground.
  - **Slow-write-1:** If the memristor substrate is under doped then single write pulse is not able to change the value of memristor from logic 0 to logic 1.
  - **Slow-write-0:** If the memristor substrate is over doped then single write pulse is not able to change the value of memristor from logic 1 to logic 0.
- **Faults caused by transistor defects**

When the transmission gate on either side of a memristor cell is stuck-open then the equivalent resistance of memristor is very high, thus read data is always at logic 0. On the other hand, when the transmission gates on both the sides of memristor are stuck-on then memristor is always selected irrespective of the value on write lines. It results in sneak path current thereby causing Incorrect Read Fault and Write Disturbance Fault.

- **Faults caused by defects in connecting wires**
  - Write Disturbance Fault:

Suppose W0′-W1′ is shorted. When memristor cell C(1,0) is selected for writing operation then W1=1, W1′=0 and for the cells in other rows WRITE=0 and $(WRITE)^{-}$=1. But due to AND bridging between W0′ and W1′ value on W0′ is forced to logic 0. Thus, memristor cell C(0,0) is unwantedly selected through PMOS and write operation is unnecessarily performed on it. These results in a WDF (write operation performed on aggressor cell disturbs the value of victim cell).

- Incorrect Read Fault:

Let W0′-W1′ is shorted. If memristor cell C(1,0) is selected for read operation then short pulse is applied to W1 and W1′ and for the cells in other rows WRITE=0 and $(WRITE)^{-}$=1. But due to AND bridging between W0′ and W1′ value on W0′ is forced to logic 0. Thus, memristor cell C(0,0) is unwantedly selected through PMOS. It results in IRF (read operation results in an incorrect read value despite correct value stored in it).

- Stuck at Fault:

Suppose D0-D1 is shorted and write 1 operation is to be performed on memristor cell C(0,0) so W0 = 1, W0′=0 D0=1, D0′=0. Value on data lines of all other columns should be 0. But due to AND bridging between D0 and D1 value on D0 is forced to logic 0. Thus, write 1 operation is not performed correctly, resulting in SA0 fault.

Table 2 summarizes bridging defects and their fault models.

IV PROPOSED MARCH ELEMENT FOR 2TG1M MEMORY

To detect the faults for 2TG1M memristor memory defined in section III, March test is proposed. The March sequence, March-2TG1M is as below.

March-2TG1M: {M1 : ⇳ (w1); M2 : ⇑(r1,w0,r0); M3 : ⇑ (r0,w1); M4 : ⇓ (r1,w0) ;M5 : ⇓ (r0,w1)}

To easily understand the algorithm, each March element has been labelled with “Mx”, where x ∈ {1, 2,... }.

⇑, ⇓, or ⇳ indicates that the memory addressing sequence is ascending, descending, or either. Subsequently, how the March-2TG1M detects the defined 2TG1M faults is as below.

- SA0F: it is sensitized by M1 and detected by first read operation of M2.
- SA1F: it is sensitized and detected by M2.
- IRF: it can be sensitized and detected by same tests as that for stuck-at-faults i.e. M1, M2.
- Slow-write0: it is sensitized by M1 and w0 of M2 and detected by r0 of M2.
- Slow-write1: it is sensitized by w0 of M2 and w1 of M3 and detected by r1 of M4.
- WDF: WDF(0,0) whose aggressor position is lower than the victim are sensitized and detected by M1 and r1, w0 of M2; WDF(0,0) whose aggressor position is higher than the victim are sensitized and detected by w1 of M3 and M4; WDF(1,1) whose aggressor position is lower than the victim are sensitized and detected by w0 of M2 and M3; WDF(1,1) whose aggressor position is higher than the victim are sensitized and detected by w0 of M4 and M5.

For an mxn 2TG1M memory, March-2TG1M needs 5mn read operations as well as 5mn write operations.

V CONCLUSION

In this, paper detailed fault analysis for mxn 2TG1M memristor memory is done. The advantages of 2TG1M structure over 1T1M structure come along with some additional bridging faults. Thus, 2TG1M memory structure increases memory speed on the cost of increase in testing efforts. Analysis of fault models like stuck-at, slow write, incorrect read and write disturbance are carried out. The March Test proposed comprehensively covers all defined faults and is based on analysis of previous work carried out on memristor memories. The proposed March Test requires 5mn read and 5mn write operations for mxn 2TG1M memory.

Table 2: Fault Types Caused by Bridge Defects

Defect Location	Aggressor	Victim	Fault Models
R_{B1}	C(b,0)	C(1,0)	WDF(1,1), WDF(0,0)
		C(b,0)	IRF
R_{B2}	C(0,0)	C(1,0)	WDF(1,1), WDF(0,0), IRF
	C(1,0)	C(0,0)	
R_{B3}	C(a,0)	C(0,0)	WDF(1,1), WDF(0,0)
		C(a,0)	IRF
R_{B4}	C(b,0)	C(0,0)	WDF(1,1), WDF(0,0)
		C(b,0)	IRF
R_{B5}, R_{B15}		C(0,0)	SA0
R_{B6}, R_{B19}		C(0,0)	SA1
R_{B7}		C(a,0)	SA0
R_{B8}		C(a,0)	SA1
R_{B9}		C(0,0)	SA0
		C(a,0)	IRF
R_{B10}		C(0,0)	SA1
		C(a,0)	IRF
R_{B11}, R_{B16}		C(0,0)	SA0
		C(0,1)	SA0
R_{B12}, R_{B18}		C(0,0)	SA0
		C(0,1)	SA1
R_{B13}, R_{B20}		C(0,0)	SA1
		C(0,1)	SA0
R_{B14}, R_{B22}		C(0,0)	SA1
		C(0,1)	SA1
R_{B17}	C(0,0)	C(1,0)	WDF(0,0)
		C(0,0)	IRF
R_{B21}	C(0,0)	C(1,0)	WDF(1,1)
		C(0,0)	IRF

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